SOLID STATE IMAGE SENSOR

Field of the Invention

[0001] The present invention relates to image sensors, and in particular, to solid state image sensors with active pixels.

Background of the Invention

[0002] As is well known, in active pixel image sensors an area of the pixel acts as a photodiode, with photon-generated current being integrated on the self-capacitance of the photodiode. This charge is essentially an analog representation of light received at that pixel during the exposure period. When a digital signal is desired, it is necessary to provide A-D conversion.

[0003] Most active pixels use one or more A-D converters located off the image plane. This maximizes the light-converting properties of the image plane, but at the expense of requiring a relatively complex switching or multiplexing arrangement to transfer pixel signal values to the A-D converters.

[0004] Layouts have been proposed in which each pixel has its own A-D converter; see for example U.S. Patent Nos. 5,461,425 and 5,801,657 to Fowler et al., U.S. Patent No. 6,271,785 to Martin, and IEEE Journal

Solid State Physics, December 2001, Vol. 36, No. 12, p. 2049 (Kleinfelder et al). However, these layouts have a disadvantage in that the additional circuitry in each pixel severely reduces the ability of the pixel to collect photon-generated electrons, and thus severely reduces sensitivity.

Summary of the Invention

[0005] The invention is defined in claim 1.

[0006] Preferred features and advantages of the present invention will be apparent from the other claims, and from the following description.

Brief Description of the Drawings

[0007] Embodiments of the invention will now be described, by way of examples only, with reference to the drawings, in which:

[0008] Figure 1 illustrates a pixel in a prior art image sensor;

[0009] Figure 2 is a circuit diagram showing one use of the pixel of Figure 1;

[0010] Figure 3 illustrates a pixel in an image sensor according to one embodiment of the invention;

[0011] Figure 4 is a circuit using the pixel of Figure 3;

[0012] Figures 5 and 6 are timing diagrams illustrating operation of the circuit of Figure 4;

[0013] Figure 7 is a timing diagram for a modified mode of operation of the invention;

[0014] Figure 8 is a timing diagram showing a further modified mode of operation of the invention;

[0015] Figure 9 shows part of the circuit of Figure 4 in greater detail;

[0016] Figure 10 shows an alternative circuit to the circuit of Figure 9; and

[0017] Figures 11, 12 and 13 respectively show modifications to the circuit of Figure 4.

Detailed Description of the Preferred Embodiments

[0018] Figure 1 shows a prior art approach to an image sensor having in-pixel circuitry such as an A-D converter. The sensor is formed on a P-type epitaxial layer 12 overlying a P-type substrate 10. The top part of the P-type epitaxial layer 12 is doped to provide the circuit components, namely an N-well 14 forming a collection node, NMOS transistors in a P-well 16, and PMOS transistors in an N-well 18.

[0019] For correct operation, the P-well 16 is biased to Vss (ground/0V), and the N-well is biased to Vdd, typically 3.3V or 1.8V. The collection node 14 is biased to a voltage between Vss and Vdd.

[0020] Light is absorbed by the silicon at a depth which is wavelength dependent. Typically, visible light generates a substantial number of electrons at a depth that is greater than the wells 14, 16 and 18. The collection node 14 as shown in Figure 1 will collect electrons that are generated directly beneath it. The electrons which are generated close to the border of the collection node 14 and the P-well 16 are attracted to the positive potential of the collection node 14 and are collected. However, the electrons which are generated underneath or close to the N-well 18 are attracted to the positive bias of the N-well and are not collected. This corresponds to a loss of sensitivity of the pixel.

[0021] Figure 2 illustrates a circuit of the sensor of Figure 1. One pixel 20 is shown, which includes the collection node 14 shown as the equivalent diode 22 and capacitance 24. NMOS transistors M1-M4 control operation of the pixel, as will be described in more detail below. A comparator is formed by PMOS transistors M5-M7 and NMOS transistor M8, and provides an output on line 26 when the sampled pixel voltage equals a ramp voltage Vramp on line 28.

[0022] A number of schemes are possible for using the change of state of the comparator. In the example shown, the line 26 sets an N-bit latch 30 according to a 10-bit gray scale. The latch 30 could be inside or outside the pixel 20. The latch 30 for a given pixel is enabled at the appropriate time by a decode or select circuit 32. The latch 30 thus outputs a 10-bit representation of the pixel value, in this example to a frame store circuit 33.

[0023] Turning to Figure 3, the invention in this embodiment once again has a P-type epitaxial layer 10 over a P-type substrate 10. A collection node 14 is formed as an N-well. The surrounding surface is formed as a P-well 16 with amplification transistors provided by NMOS transistors only. The collection node 14 and P-well 16 may be contiguous, as shown, or may be separated by insulation or isolation material.

[0024] Thus, the sensor of Figure 3 does not contain an N-well other than the N-well forming the collection node 14. Electrons generated in the epitaxial layer 10 are attracted to the most positive point in the pixel, which is now the collection node 14, thus increasing the sensitivity.

[0025] Figure 4 shows one possible circuit making use of this embodiment. As discussed, the pixel 20 contains only NMOS transistors. Transistor M4 is used to reset the pixel voltage. Transistors M1-M3 form a long tail pair or differential amplifier, with M1 forming a current source to M2 and M3. The long tail pair is connected to a current mirror formed by PMOS transistors M5 and M6 located off or outside the pixel.

[0026] After reset, the voltage on the gate of M2 is higher than Vref (gate of M3). More current flows through M3 than M2 and hence more through M5 than M6. This keeps the gate of M7 high and the output Comp_out low.

[0027] After some time, dependent on the amount of light falling on the pixel, the voltage Vphotodiode will be lower than that on the gate of M3. When this happens, more current will flow through M3 than M2 and hence more through M6 than M5. This takes the gate of M7 low and the output Comp_out goes high.

[0028] The time that this transition takes place is stored using the N-bit latch 30 (in this example a 10-bit latch is used). In the arrangement of Figure 4, there is an external current mirror and latch for each pixel. Typically, the output of the pixel latches are connected to a bus. An address bus 31 and a select circuit 32 are used to enable the bus output.

[0029] Figure 5 illustrates the timing for the circuit of Figure 4. As will be seen at A and B, the greater the amount of light falling on the pixel, the steeper is the slope of the integrating waveform and the earlier the comparator changes state.

[0030] This arrangement has the disadvantage that, as shown at B' in Figure 6, low light levels produce a

very shallow slope on Vphotodiode. This can be addressed either by lengthening the integration time which reduces the speed of the whole system, or by setting Vref very close to the maximum of Vphotodiode which makes the system very sensitive to noise. Figure 7 overcomes these limitations by providing Vref in the form of more than one linear ramp C during integration.

[0031] Figure 8 illustrates a further modification for use in reducing fixed pattern noise. With a careful layout, transistors M2 and M3 will match accurately. However, there is likely to be an offset when the outputs from the long tail pair and the current mirror change states. Moreover, because of manufacturing tolerances this offset is likely to vary between pixels, causing fixed pattern noise.

[0032] Figure 8 shows an offset cancellation scheme. Reset transistor M4 is kept closed and the pixel is kept in reset. A ramp D is applied to Vref at the gate of M3. The system operates in a similar manner to the exposure of the pixels. When the comparator changes state the latch stores the count value on the Gray(0...9) bus. This count is stored in the frame store circuit 33 for subsequent subtraction from the output of the integration phase.

[0033] In a straightforward implementation, the width of the frame store function matches the width of the latches and the gray scale counter, i.e., 10 bits in the present example, as seen in Figure 9. However, to save space in the IC it is possible to use a narrower width frame store function, and a selector circuit so that only the most relevant 8 bits, for example, are used. This is illustrated in Figure 10 where a multiplexer 36 is used to select the 8 most

significant bits if the signal is large, or the least significant 8 bits if the signal is small.

[0034] The foregoing description assumes that each pixel has its own current mirror and latch. This is feasible for small arrays, but for larger arrays it becomes necessary to share the current mirrors and latches between many pixels. In the system shown in Figure 11, the Bias1a/Bias1b signal to the current load in the long tail pair is used to enable each of the rows in sequence. When Bias1a/Bias1b is low the pixel's readout is disabled, enabling the pixel to set to a suitable level. When Bias1a/Bias1b goes high the long tail pair is enabled and the difference between the photodiode voltage and Vref is output as a current difference on lines 38 and 40. The control signal for Bias1a/Bias1b is added to the address bus PixA(0...9) so that the output from the latch is written into the appropriate memory location.

[0035] For larger arrays, the parasitic effect of the drains from all the pixels in the column will slow the access. To avoid this, as illustrated in Figure 12, NMOS FETs 42 and 44 are inserted at each pixel into both legs of the long tailed pair and are used to multiplex the output onto the lines 38 and 40. Alternatively or additionally, cascode transistors 46 can be used (as seen in Figure 13) to reduce the effects of stray capacitance on the lines 38 and 40 from the pixels.

[0036] The foregoing embodiments have been described in terms of a P-type substrate, with the collection node formed as an N-well and only NMOS transistors formed within the pixel. In principle, this could be inverted with an N-type substrate, wherein the

collection node is a P-well and only PMOS transistors are within the pixel.

[0037] The invention provides image sensors in which the pixels have greater sensitivity than in the prior art. Also, the pixels have a balanced readout which provides greater noise immunity than in the older analog readout mechanisms. Greater sensitivity allows a sensor to operate at lower light levels, which is a significant requirement for cameras. Systems which incorporate their own light source require less power to illuminate the pixel, leading to reduced power consumption.